Amendments to the Specification:

All paragraph numbers refer to Patent Application Publication No. 2005/0175000 A1, published August 11, 2005.

Please replace paragraph [0016] with the following amended paragraph:

[0016] An alignment of all incoming cells from connected input/output means is made available according to an embodiment~~claim 2~~. In this case the transmission data rate may be at its maximum, as transmission periods only last for exactly one transmission of a cell.

Please replace paragraph [0017] with the following amended paragraph:

[0017] A central clock signal, according to an embodiment~~claim 3~~, allows easy cell synchronisation.

Please replace paragraph [0018] with the following amended paragraph:

[0018] Serialisation and de-serialisation, according to at least one embodiment~~claim 4 and 5~~, allows serialised transmission of data packets. Evaluating a bit error indicator, according to an embodiment~~claim 6~~, may also be carried out based on a coding scheme applied for transmission on a transmission line. The output of the bit error indication may be used as decision to change the offset of start of cell times in order to delay the output of cells.

Please replace paragraph [0019] with the following amended paragraph:

[0019] Using an offset counter, according to an embodiment~~claim 7~~, allows a shift of the start of cell times of outgoing cells with respect to a matrix configuration synchronisation signal. The delay is incremented or decremented by defined step widths.

Please replace paragraph [0020] with the following amended paragraph:

[0020] The offset counter may also be controlled, according to an embodiment~~claim 8~~, in a way that the start of cell time is pre-running with respect to the start of cell signal as much as possible without generation of bit errors, and afterwards delaying the start of cell time as much as possible until bit errors occur. The length of cell transmission periods may then be adjusted and the total throughput is increased. The bit error rate is brought to a minimum in case the start of cell time is set according to an embodiment~~claim 9~~.

Please replace paragraph [0021] with the following amended paragraph:

[0021] According to a further aspect of the invention, a packet switch is provided, where said port controller comprises a start of cell signal generator for generating start of cell signals, an offset controller for shifting a start of cell time based on said start of cell signal, and an error detection mean for detecting corrupt received cells and where said cross-connection means comprises a configuration controller for controlling an oscillation between a loopback configuration and a no-transmission configuration of said cross-connection means.

Please replace paragraph [0022] with the following amended paragraph:

[0022] A packet switch, according to an embodiment~~claim 11~~, is advantageous, as a central clock signal allows exact synchronisation between port controllers and cross-connection means.

Please replace paragraph [0023] with the following amended paragraph:

[0023] By providing serialisation and de-serialisation means, according to an embodiment~~claim 12~~, data bits or packets may be serially transferred.

Please replace paragraph [0024] with the following amended paragraph:

[0024] Providing an N × N cross matrix, according to at least one embodiment~~claims 13 and 14~~, configuration changes may be applied easily. In such a matrix, a line corresponds to an input port and a column corresponds to an output port. A switch at position (X, Y) in said N × N matrix connects input port X with output port Y.

Please replace paragraph [0025] with the following amended paragraph:

[0025] By providing a bit error indicator, according to an embodiment~~claim 15~~, a bit error may be derived from the coding scheme applied for a transmission on a line.

Please replace paragraph [0045] with the following amended paragraph:

[0045] During set-up the crossbar matrix 40 is switched between unit matrix and null matrix by configuration controller 46, which is controlled by a system clock signal generated by central clock generator 48. The system clock generated by central clock generator 48 is also provided to offset counter 32 and to start of cell signal generator 30. Cells which are retransmitted to port controller 1 are received in the de-serialiser ~~serialiser~~ 36. The received cells are evaluated in bit error rate indicator 38. In case a bit error occurred, the offset counter 32 is increased. By increasing the offset counter 32 the start of cell signal generator generates a start of cell time prevailing the central clock signal by the amount of the offset counter 32. By increasing the offset counter 32, the start of cell time will be changed until a cell is transmitted to crossbar matrix 40 and received by de-serialiser 36 without transmission errors, which means that the cell is received in crossbar matrix 40 in a transmission period.